An Ultra-Low Power 16-Bit Sigma-Delta ADC For Bio-Medical Applications

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Abstract: This paper describes an ultra low power 16 Bit second order Sigma Delta modulator for Analog to Digital converters. The proposed circuit provides a power efficient ∑Δ modulator which helps in IoT sensor applications as it is advantageous to utilize less power in sensor applications. In the process of conversion, there might be a chance of occurrence of quantisation error. In order to reduce this error, Sigma Delta modulators are used. The proposed circuit has been designed using CMOS 180nm technology in Cadence Virtuoso Tool. Second order ∑Δ ADC is fed with the supply voltage of 1V. The high resolution obtained through this circuit is advantageous for higher accuracy in Sigma processing. In the designing of ∑Δ modulator, the design of analog circuits like Operational Amplifier is also included in CMOS technology. The clock frequency of 10KHz has been used in this circuit. It achieves an SNDR of 69 dB and SNR of 145.39 dB. The oversampling rate for the proposed circuit is 1024. The power consumption obtained for the second order Sigma Delta ADC is 41.27 µW at a sampling frequency of 10KHz.

Keywords: Op-amp, Integrator, Subtractor, Comparator, D-Flipflop, 1-Bit DAC.

I. INTRODUCTION

ADCs are mainly used in the applications of sensors. The sensor applications require very high accuracy and linearity. They also require very low offset voltage and noise. The major consideration in ADC is low power. In our proposed circuit, the main concentration is about maintaining the low power requirements without sacrificing performance and reliability.

![Block Diagram of ADC](image)

Fig. 1: Block Diagram of ADC.

Fig.1 shows the block diagram of ADC. In this, the analog input fed for ADC will be continuous in time and amplitude. The digital output obtained will be of discrete in time and amplitude.

There are two types of ADCs available: Nyquist rate ADCs and Oversampling ADCs. Sigma Delta Analog to Digital Converter comes under the category of Oversampling ADCs. Out of the ADCs available, Sigma Delta ADC is used, as it oversamples the input signal reducing the requirement of anti-aliasing filters.

Same as oversampling ADCs, Sigma Delta ADCs also samples the signal at an over sampled frequency of

\[ f_N = \frac{k}{2F} \]  

Equation (1)

where, k is oversampling ratio which can be given by \( k = \frac{f_m}{F} \)

The other feature of Sigma Delta Modulator is that it acts as an Integrator for signal but as a Differentiator for noise, hence, pushing noise to higher level frequencies.

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The noise power reduction in those frequencies means, that, it gives a higher Signal to Noise ratio (SNR). The increase in SNR results in greater effective number of bits of resolution in ADC.

II. ARCHITECTURE AND OPERATION

The analog to digital converters can be classified as; Flash, SAR and Oversampling type. Sigma Delta ADC comes under oversampling type ADC, which is different when compared to conventional type ADCs such as Flash and SAR. The conventional ADCs operate at Nyquist Rate whereas oversampling type i.e., Sigma Delta ADCs operate at high oversampling rate.

In the Sigma Delta Modulator based ADC, Delta (Δ) means a small incremental change or deviation and Sigma (∑) means summation or integration. In designing of Sigma Delta ADC, the complexity of the system decreases because of the reduced need of multi-bit ADCs for conversion process. The main trade-offs in designing of Analog to Digital converters is its speed of conversion and resolution. Sigma Delta ADC is used as it shows high performance compared to all other ADCs.

(i) First order Sigma Delta ADC:

Fig. 2 represents the first order Delta Sigma ADC in block format. Here, a single Integrator is used which is designed using operational amplifier.

![Fig. 2: First order Sigma Delta ADC.](image)

Here, analog signal with input frequency of 10KHz is fed to the subtractor as input signal. The output of subtractor is fed as input to the integrator. Integrator output is given as input to the comparator whose output is fed to the D Flipflop. D Flipflop is connected with an external clock with a clock voltage of 1V. 1Bit DAC is connected in feedback whose output is fed back to the negative input of subtractor. The first order Sigma Delta ADC is observed to obtain the power consumption of 21.94µW for a supply voltage of 1V.

(ii) Second order Sigma Delta ADC:

Fig. 3 represents the second order Sigma Delta ADC in block format. Second order Sigma Delta ADC provides better stability and also better noise immunity when compared to first order Sigma Delta ADC.
The block diagram of proposed circuit consists of Subtractor, Integrator, Comparator, D-flipflop, 1-Bit DAC. Among these blocks, subtractor, integrator and comparator fall under analog circuit whereas the latch(D-flipflop) and 1-Bit DAC falls under digital circuit. The analog circuit is designed using an Operational amplifier because of its advantage of high performance.

A) SUBTRACTOR:

![Subtractor Diagram]

Fig. 4: Subtractor

Fig. 4 represents the block diagram of Subtractor used in Sigma Delta ADC. A subtractor does subtraction operation which is one among the basic level binary operations. It can also be utilised to represent many binary bits. If $V_1$ is higher, then the output will be negative. If $V_2$ is higher, the output will be positive.

B) INTEGRATOR:

![Integrator Diagram]

Fig. 5: Integrator
Fig. 5 represents the block diagram of Integrator. The integrator that is designed using operational amplifier performs integration operation w.r.to time. Its output voltage is in proportion with the time integrated input. The integrators are mostly used in ADCs, Analog computers and also in wave shaping circuits.

C) COMPARATOR:

![Comparator Diagram]

Fig. 6: Comparator

Fig. 6 represents the block diagram of comparator. The comparator generally compares the two input voltages and provides an output either 0 or 1 based on the comparison result. It also uses operational amplifier in its schematic. The comparator produces an output 1 if the non-inverting terminal is higher than the inverting terminal and produces an output 0 for the other case.

II. SIGMA DELTA ADC

As presented in Fig.3, the second order Sigma Delta ADC consists of 7 blocks for which the symbols are created by pre-testing using a test circuit. There will be two types of Sigma Delta ADCs. They are Continuous time Sigma Delta ADC and Discrete time Sigma Delta ADC. Here, Discrete time Sigma Delta ADC is used which can operate at a desired clock frequency. The sinusoidal input is fed to the Subtractor’s positive terminal and also the feedback is connected to the negative terminal of the subtractor. The output of subtractor is fed as input to the integrator and the integrator output is fed to the next subtractor and so on. The output of the comparator is fed to D-Flipflop where, the D-Flipflop performs the delay operation for the fed input and produces a bit-stream output. Now, this output from D-Flipflop is fed as input to the feedback element.

The feedback element used in this circuitry inverts the output and feeds to the negative terminal of the subtractor. This process continues to obtain a low noise output for the converter.

In this proposed circuitry, second order Sigma Delta ADC is used, as, when compared to first order, it shows greater accuracy.

![Test Circuit Diagram]

Fig.7: Test circuit of second order ∑Δ-ADC.
There will be a slight increase in the power consumption from first order to second order because of the number of components utilised to design the circuit. But, in terms of performance, accuracy and applications, the second order Sigma Delta ADCs shows many advantages. Among the ADCs available, ∑∆-ADC shows high speed of operation and better noise shaping. Because of the use of 180nm technology, it works on low power. The ∑∆-ADCs are highly reliable and also they can help to reduce the cost of fabrication.

The ENOB defines the effective resolution in bits for a system. ENOB can be calculated using the formula,

\[
ENOB = \frac{SNR-1.76}{6.02} \text{ dB}
\]

The 1.76 indicates the quantization error for an ideal ADC.

The 6.02 indicates the conversion from decibels to bits.

The ENOB can also be measured as a quality measure in case of sample and hold amplifiers.

- **DESIRED SPECIFICATIONS**

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<th>S. No</th>
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<td>Technology</td>
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<tr>
<td>2</td>
<td>Power supply</td>
<td>±1V</td>
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<tr>
<td>3</td>
<td>Input signal</td>
<td>Upto 2.5KHz</td>
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<tr>
<td>4</td>
<td>Input clock</td>
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<td>Gain</td>
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<td>7</td>
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<td>10</td>
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<td>11</td>
<td>Power</td>
<td>41.27µW</td>
</tr>
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</table>

III. **PARAMETERS OBTAINED**

When compared with SAR or other types of ADCs, the Sigma Delta ADCs shows high performance in terms of performance, accuracy and resolution. The gain of the op-amp used in designing the blocks of Sigma Delta ADC is obtained as 81.07 dB. The power consumption obtained for the second order ∑∆-ADC was 52.6µW, whereas for first order, it is observed to be 21.94µW. As the circuit is designed for the applications of IoT sensors, the sensors used in those areas require high accuracy also by maintaining the power consumption.

IV. **COMPARISON TABLE**

Table 2: Comparison Table.

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<tr>
<td>1</td>
<td>Technology</td>
<td>180nm</td>
<td>180nm</td>
</tr>
<tr>
<td>2</td>
<td>Power supply</td>
<td>±900mV</td>
<td>±1V</td>
</tr>
<tr>
<td>3</td>
<td>Input signal</td>
<td>Upto 500KHz</td>
<td>Upto 2.5KHz</td>
</tr>
<tr>
<td>4</td>
<td>Input clock</td>
<td>250 KHz</td>
<td>250 KHz</td>
</tr>
</tbody>
</table>
The Sigma Delta ADC has been fed with a DC operating voltage of 1V. The measure of dynamic range for an ADCs would be defined by their Effective number of bits (ENOB).

### V. SIMULATION RESULTS AND DISCUSSION

![Simulation results for second order ∑Δ-ADC.](image)

The simulated result for the Sigma Delta based Analog to Digital converter is as shown above. The input given is a sinusoidal signal. When a sinusoidal input is fed to the system, the output Vout is a pulse signal. Voutbar is the inverted output of Vout.

### VI. CONCLUSION

The power consumption for the proposed circuit was observed to be minimum for a supply voltage of 1V. Even though the first order Sigma Deltamodulator for ADC shows the power consumption of 21.94µW, the second order is advantageous as it shows high performance in terms of accuracy also by maintaining the consumption of power, which is the main requirement of IoT sensors. Hence, the second order Sigma Delta ADC can be used in the applications of IoT sensors. Further, the performance of the proposed circuit can be improved by increasing the number of bits. The OSR(Over Sampling Rate) was observed to be 1024 with SNR of 145.39 dB. The resolution is 16- Bit which is high and advantageous for all practical applications. The second order Sigma Delta modulator for ADC is observed to be 41.27 µW. The Application of design is Bio-Medical.

### VII. REFERENCES


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