SEQUENTIAL LOGIC GATES USING QUANTUM DOT CELLULAR AUTOMATA FOR HIGH SPEED APPLICATIONS

AMAN KUMAR1, Dr. SUBHASHISH BOSE2
1Research Scholar, Dept. of Electronics and Communication Engineering, Sri SatyaSai University of Technology & Medical Sciences, Sehore, Bhopal-Indore Road, MadhyaPradesh, India
2Research Guide, Dept. of Electronics and Communication Engineering, Sri Satya Sai University of Technology & Medical Sciences, Sehore, Bhopal-Indore Road, MadhyaPradesh, India

1. ABSTRACT
Quantum-dot Cellular Automata (QCA) is an extremely intriguing nano-scale innovation. Tiny component size and super low power utilization are the main highlights of QCA contrasted with CMOS. Counters are considered as perhaps the most essential segments in successive circuits. As indicated by the high pace of measurements shrinkage in customary CMOS circuits, serious challenges threat this technology. An effective design for irregular access memory cell with set and reset capacity which depends on the D-hook. Planning powerful and proficient QCA-based consecutive circuits is a critical subject which needs efficient designs for locks. Quantum-dot cellular automata (QCA) is quite possibly the most encouraging nanotechnologies that empower territories of more modest size, for example 60% less plan region than the CMOS innovation, with ability to create fast by taking less cycles contrasted with the other CMOS plans with decrease scaling issues. The QCA-based plans are considered as the best elective answers for the semiconductor based (CMOS) plans. This paper assesses the exhibition of performance of various implementations of Sequential logic gates QCA based XOR and NAND gates and Reversible logic gates QCA based Feynman gate and Fredkin gate proposes different novel formats with better execution boundaries. The QCA permits more conceivable plan structures for every logic gate to empower enhancement of the zone. These constructions are planned and reproduced utilizing QCA Designer Tool.

Keywords: Quantum-dot cellular automata (QCA), nano-scale technology, XOR and NAND gates, CMOS

2. INTRODUCTION
In the present technological period CMOS is the administering innovation in very large scale integration (VLSI) frameworks. Nonetheless, as size of the semiconductor is contracting, issues like high spillage current, high lithography cost, power utilization and limit of speed in GHz are emerging. Thus, we need some elective innovation which can substitute CMOS, winning preferred properties and execution over CMOS. A standout amongst other plausible choices is mix of reversible logic and quantum dot cellular automata (QCA). These are the arising innovations which can be utilized for super low force nano-circuits. QCA is a one of a kind nanotechnology which guarantees ultra low power, particularly thick and high velocity setup for executing any logical capacity at nano-scale. In addition the traditional logic circuit scatters warmth of the request KTln2 joule for each piece lost in calculation, where K is Boltzmann's steady and T is supreme temperature. This heat dissipation happens in irreversible circuits and can be wiped out by presenting reversibility in the circuit. Reversible logic circuits discover various applications in low force VLSI, quantum processing, optical and DNA computing. Numerous examinations have been done on reversible combinational circuits yet there is extension to investigate reversible successive circuits. Lately, numerous examinations have been accounted for on plans of reversible flip failures, counters, registers, and memory cells. QCA cells perform calculation by connecting coulombically with adjoining cells to impact each other's polarization.
2.1 QCA Basic Cell

QCA circuits are made out of indistinguishable segments which are alluded to as QCA cells. A QCA cell, a square-shape structure, has four dots situated at the four corners and two stacked electrons which are permitted to move between the Dots (Figure 2.1). Because of Coulombic repellant power, the electrons possess the dots situated at the slantingly gone against corners. The major construction in quantum dot cellular automata is a QCA cell which is a squared cell with four quantum dots set at its corners and two free electrons. These electrons can tunnel quantum precisely by balancing burrow hindrances among dots and gather askew because of Coulombic shock. Every cell addresses somewhat through a proper design of charge. The Quantum-dot relates to a little semi-transmitter nano-construction or metal-islands with a width of 2-10 nm. The two portable electrons can move to various Quantum-dots in the QCA cell by methods for electron tunneling.

![Figure 2.1: QCA cell with four Quantum-dots](image)

2.1.1 QCA gates

The elementary gates in QCA configuration are majority gate and an inverter as demonstrated in Figure 2.2. A majority gate is acknowledged with five QCA cells with three inputs and one output. It takes contribution from three cells and gives choice on the fourth cell. The output depends on the majority of information cells. Assuming majority of input cells are polarized as logic 1, yield of the gate is additionally 1.

![Figure 2.2 Majority gate](image)

The majority gate realizes a three-variable logic function as follows.

\[
M(A, B, C) = AB + AC + BC
\]  

Equation (2.1) addresses the fundamental Boolean function for majority gate, utilizing which fundamental capacities like logical and logical OR can be carried out by fixing one input to logic 0 or 1, separately. Another essential gate is inverter as demonstrated in Figure 2.3. Assuming the cells are put at 450, yield is supplement of the information understanding an inverter. This way every one of the essential gates and henceforth all inclusive gates can be carried out utilizing majority gates and QCA inverter.

![Figure 2.3. QCA inverter](image)

2.1.2 Cell-to-Cell Response

The cell-to-cell reaction work is appeared in Figure 2.4. It outlines that the idea of the reaction is exceptionally non-straight for example a feeble polarization of one cell causes a solid polarization of the adjoining cell. This suggests that, in a wire, if the driver or any of the moderate cells has a feeble polarization, the ensuing cell would
in any case get emphatically captivated. This conduct compares to a cradle reestablishing a sign worth to the inventory voltage in customary computerized circuits. This conduct is alluring for imperfection resistance in QCA circuits where one cell may not get strongly polarized because of position issues yet would in any case bring about solid polarization in neighboring cells.

Figure 2.4: Nonlinear cell-to-cell response
A driver of a QCA cell could be an info gadget like a nanotube, an extremely slim wire or a tip of a checking scanning tunneling microscope (STM). In semiconductor QCA, a standard strategy called "plunger electrode" has been utilized to adjust the electron inheritance of the info cell. Perusing the yield condition of a QCA cell is troublesome, in light of the fact that the necessary estimation measure should not change the charge of the yield cell. Electrometers produced using ballistic point-contacts, the scanning tunneling microscope strategy and SET electrometer have been utilized to peruse the yield. Dissimilar to ordinary logic circuits in which data is moved by electrical flow, QCA works by the Coulombic collaboration that interfaces the condition of one cell to the condition of its neighbors.

2.2 QCA Wires
For signal engendering in QCA circuits wires assume an essential part. A wire can be utilized to propagate signal from contribution to the yield. The data transmission in a QCA wire happens by Coulombic power. At the point when an info is applied to the info cell, the double data propagates from left to one side because of the Coulombic shock between the electrons of adjoining cells. At the point when all cells in the wire settle down to the ground states, they have a similar polarization. Any cell along the wire that is antipolarized with the information would be at a higher energy level, and would before long settle down to the right ground state. Various strategies have been investigated to handle the issue of wire intersections in QCA.

2.2.1 90-Degree QCA Wire
Figure 2.5 shows how a paired worth propagates down the length of a QCA wire. A 90-degree wire is a flat column of QCA cells. The twofold sign propagates from left-to-right in view of the Coulombic interactions between cells.

Figure 2.5. Interaction between the cells in 90° QCA wire
In Figure 2.5. Double '0' (from polarization $P = -1$) will propagate down the length of the wire due to the Coulombic communication between the cells. At first, the electron repulsion brought about by Coulombic connection between cell 1 and cell 2 will make cell 2 change polarizations. At that point, the electron repugnance between cell 2 and cell 3 will make cell 3 change polarizations. This interaction will proceed down the length of the QCA wire.

2.2.2 45-Degree QCA Wire
Standard 45-degree QCA wire involves cells arranged at 45-degree cells. It is gotten by turning the direction of 90-degree. Nonetheless, assuming a wire is framed utilizing 45-degree cells, it brings about an Inverter chain as demonstrated in Figure 2.6. To comprehend the sign proliferation of 45-degree cells, accept that the information
cell is at logic one (P = +1), with the 45-degree direction. As the double worth propagates down the length of the wire, it shifts back and forth between polarization P = +1 and polarization P = -1, on the other hand. A modified or un-supplemented worth can be ripped off the wire by setting a ripper cell at the appropriate area thinking about the heading of sign engendering. The huge benefit of the 45-degree wire is that both the sent worth also as its supplement can be acquired from a wire.

![Image](image.png)

**Figure 2.6. A 45° QCA wire**

3. LITERATURE REVIEW

*HemaSandhyaJagarlamudi et al (2020):* The utilization of Quantum dots is a promising arising Technology for executing advanced framework at the nano level. It is proficient for alluring highlights like quicker speed, more modest size and low force utilization than semiconductor innovation. In this paper, different Combinational and consecutive logical constructions - HALF ADDER, SR Latch and Flip-Flop, D Flip-Flop going before NAND, NOR, XOR, XNOR are examined dependent on QCA plan, with similarly less number of cells and region. By applying these formats, the equipment prerequisites for a QCA configuration can be decreased. These constructions are planned and reproduced utilizing QCA Designer Tool. By exploiting the exceptional highlights of this innovation, we can make total circuits on a solitary layer of QCA. Such Devices are required to work with super low force Consumption and extremely high rates.

*Mohammad Mohammadi et al (2020):* This paper clarifies about a productive plan of full adder in quantum-dot cellular automata (QCA) innovation. The full adder circuit is an essential unit in computerized number-crunching and logic circuits. In this paper an improved full adder in QCA innovation is proposed. This plan is impressively declined regarding cell numbers and zone, contrasted with other full adders and postponement is kept at least. To plan this full adder an alternate definition for aggregate and carry yields of full adder has been utilized. The reproduction brings about QCADesigner programming affirm that the introduced circuit functions admirably and can be utilized as a superior plan in QCA innovation. At last, the proposed QCA full adder is utilized to make three sizes of ripple carry adders (RCA) and satisfactory outcomes are accomplished.

4. PROPOSED METHODOLOGY

Latches and flip-flops are the fundamental components for putting away data. One hook or flip-lemon can store the slightest bit of data. The primary distinction among latches and flip-flops is that for latches, their outputs are continually influenced by their inputs as long as the enable signal is stated. In other word, when they are empowered, their substance changes promptly when their inputs change. Flip-flops, then again, have their substance change just either at the rising or falling edge of the empower signal. After the rising or falling edge of the clock, the flip-flop content remaining parts consistent regardless of whether the input changes. There are fundamentally four primary kinds of latches and flip-flops: SR, D, JK and T. The significant contrasts in these flip-flops are the quantity of inputs and how they change state.

4.1 QCA for High speed application

The key closeness of the RAM cell to the hook, it very well may be built dependent on one of the four sorts of latches. In this part, a novel and effective plan for irregular access memory cell with set and reset capacity is proposed. The offered memory cell uses two control signals (set and reset) which have a critical job for accomplishing arbitrary access memory's tasks. This plan is coordinated in the three method of activity, which entitled by Normal mode, Set mode and Reset mode.

As it is outlined in Figure 4.1(c), this plan is made out of five 3-input majority gates. The entirety of the referenced majority gates in QCA execution have a strong design concerning the streams heading that prompts more commotion insusceptibility of the circuits. One of these 3-input majority gates that is set at the output of the circuit and determined with various plan utilizes the introduced. As noted before, fundamental segment of this engineering is D-lock, so we named this design "D latch RAM". In the initial step, the stripped down adaptation of the RAM which is D-latch is represented. At the point when the Enable pin is initiated by "1", as indicated by the input signal worth, the output of the lock will be changed. By setting it to the twofold estimation of "0" or "1", substance of the lock will change to "0" or "1", separately (Figure 4.1(a)). In the subsequent advance, compose and read control circuits are added to the D-lock and set and reset signals are relegated to the memory cell in an
inventive manner (Figure 4.1 (b)) and the select sign is included the third step (Figure 4.1 (c)). Full activities of the PDRAM cell will be acquired, as demonstrated in Table 1. During the ordinary mode (Set="0" and Reset= "1"), when the select sign is high regarding Write/Read sign, Write and Read tasks will be performed. It is additionally essential that by arranging the referenced control circuit at the output point of D-lock (which appeared by Mloop in the Figure 4.1 (c)) D latch RAM circuit is upgraded for more proficient use in the bigger exhibit of RAM cells. Set and Reset signals are considered to decide the estimation of the cell by "1" and "0", individually.

Figure 4.2 shows the QCA execution of D latch RAM. This design is made utilizing three layers with advanced burned-through cells and region occupation in contrast with the cutting edge. Also, extra cells have been applied to the inputs signals for synchronization of introduced RAM. As demonstrated in Figure 4.2, every single one of the red squares which are arranged close to the input signals show the situation of the input cells as per different cells dependent on the layers. Besides the sign engendering bearings are illustrated using arrows with different colors, for example Select cell is put in the main layer and red bolt show its spread heading.
4.2 Sequential Logic gates using QCA for high speed application

4.2.1 XOR Structures

Exclusive OR, otherwise called Exclusive disjunction and represented by XOR, is a logical procedure on two operands that outcomes in a logical estimation of valid if and just in the event that one of the operands, however not both, has an estimation of valid. This structures a major logic gate in numerous tasks. A XOR gate can be inconsequentially built from a XNOR gate followed by a NOT gate. We can develop a XOR gate straightforwardly utilizing AND, OR and NOT gates. Be that as it may, this methodology requires five gates of three various types. Logically, the exclusive OR (XOR) activity can likewise be executed by the gate game plans to follow. For example they can likewise be executed utilizing NAND or NOR gates as it were. Each Boolean function can be worked from (binary) Fred kinfolk Gates (FGs), to such an extent that it has two inputs A, B and one output Y. The main plan depends on Equation (4.1) which can be improved as

\[ Y = (A + B)' . A + (A + B)' . B \]

\[ Y = (A' + B') . A + (A' + B') . B \quad (4.1) \]


\[ Y = A' . B + A . B' \]

The QCA XOR gate has no crossovers and has cell count of 34 cells and an area of approximately 0.06 um² which is less as compared to conventional layouts.

4.2.2 NAND gate structure

NAND is another general logic function, which can help execution of any logic function. AND gate followed by an inverter is the NAND. The basic symbol of NAND gate is appeared in Figure 4.4 (a). Two unique polarizations (NAND and TNAND) have been utilized to plan distinctive NAND gates dependent on the QCA, and formats of the plans are introduced in Figure 4.4(b) (I) and (ii). The Boolean expression for the output of the NAND gate is given by AND gate output followed by an inverter as demonstrated in Equation (4.2)

\[ Y = \overline{AB} \quad (4.2) \]
4.3 Reversible Logic Gates using QCA for high speed application

There are three major design goals in reversible logic: 1) The quantum cost, which is the number of 1*1 and 2*2 reversible calculations necessary to generate the logical output, should be minimized in order to reduce the computation complexity of the device. 2) The delay, which is the logical depth of the device, should be minimized. 3) The ancillary inputs and garbage outputs - inputs and outputs not implemented in the design of the gate and only serve to maintain reversibility of the device — ought to be reduced and ideally eliminated.

4.3.1 Feynman Gate

The 2*2 gate is a Feynman gate & is also called as controlled NOT, it is widely used for fan-out purposes. The inputs (A, B) and output P=A, Q=A xor B. It has quantum cost one. The Equations are:

\[
P = A \\
Q = A \oplus B
\]  

(4.3)

Figure 4.5 (a) Feynman gate (b) Implementation of Feynman Gate in QCA

4.3.2 Fredkin Gate

The Fredkin gate is a 3*3 gate, maps inputs (A, B, C) to outputs (P=A, Q=A \cdot B+A \cdot C, R=AB+A' \cdot C) having quantum cost of 5 and it requires two dotted rectangle. Fredkin gate and its quantum implementations are shown below:

Figure 4.6 (a) Fredkin gate (b) Quantum implementation of Fredkin gate

5. RESULTS

We have carried out two sorts of successive logic gate and reenacted utilizing 2.0.3 QCA creator. The usefulness of the circuit is checked from the recreated waveform. The geography of the QCA format characterizes the connection of the cells and consequently the usefulness of the general circuit. All traditional logic gates can be built utilizing QCA cells. The majority gate is the fundamental square of QCA circuits. The consequences of reproduction for all blends of A, B, and C inputs are appeared in Figure 5.1. Reproduction results affirm that the proposed QCA full adder functions admirably and demonstrate fitting execution. As an example, for inputs of A = 0, B = 1 and C = 0, the right outputs of convey = 0 and whole = 1 are produced as exhibited in Figure 5.1.
Figure 5.1. Simulation result of D latch RAM showed in 4.2

The simulations consequence of the D hook memory is shown in Figure 5.1. In light of this figure, first significant output an incentive for Mloop point and output point are accomplished after 1 and 1.25 timing cycles, separately. In the Normal mode (Set= "0", Reset="1"), if Write/Read and Select sign have been enacted by "1", compose activity will be performed and input information which is indicated between two red bolts will be kept in touch with the memory cell after 1 timing cycle. Moreover, the memory cell content is communicated to the output cell in the read time as demonstrated by dark bolts. In the Set mode, which is appeared by green arrows in mentioned figure, cell esteem is changed to "1".

The Quantum-dot Cellular Automata (QCA) XOR gate reproduction results are appeared in the figure 5.2. The QCA NAND gate simulation results are shown in 5.3. The efficient designs of Quantum-dot Cellular Automata based XOR gates with diminished number of QCA cells and region. The capacity of the Exclusive OR gate has been checked by truth table.
5.1 Reversible Logic Gates Simulation Results

All the design of basic reversible logic gates were verified by using QCA Designer tool ver.2.0.3. In the bistable approximation, we use the following parameters, which are default parameters in QCA designer tool: number of samples (12800), convergence tolerance (0.001000), radius of effect (65.00nm), relative permittivity (12.900000), clock high (9.800000e-022), clock low (3.800000e-023), clock shift (0.000000+000), clock amplitude factor (2.000000), layer separation (11.500000), maximum iterations per sample. In our QCA layouts, we have the goal of workable design with compact layout.
In the presence of noise, the precision of the estimation changes essentially, given that both the abundancy and time of the edges (Figure 5.4) are influenced by the noise. It has been shown hypothetically that quantum error correction can be utilized to reestablish the ideal estimation precision within the sight of coordinated noise, as long as it isn't resemble to the sign. Noise measures acting along a similar direction as the sign (z) can't be recognized from the sign and in this way can't be focused on. In this, we investigate how well the inconvenient impact of noise in the symmetrical direction (x) can be relieved by the error correction convention. By and large, if a sign in an arbitrary direction is expected, correction of noise in x-direction as portrayed underneath will consider detecting the z-part of the sign with upgraded precision.
6. CONCLUSION

This paper investigates a productive construction of successive logic gates, for example, NAND and XOR gates utilizing QCA with diminished number of QCA cells. The reenactment results show that the proposed circuits perform well. During the plan a consideration is made to decrease the quantity of cells just as to lessen the territory. The predominance of the proposed plans over the customary designs has been demonstrated through QCA Designer instrument regarding intricacy, engendering postponement and exactness of activity. The proposed successive circuits can likewise be applied as the structure squares of bigger circuits which requires the high velocity application. These circuits are advanced and more practical than the cutting edge circuits. QCA-based plan of reversible circuits has a lower quantum cost than customary plan. The imperfection investigation is valuable for flaw free execution of the plans. The proposed consecutive logic gates can be valuable in accomplishing nanoscale, quicker, committed units of the adder for advanced sign preparing for nanocorrespondence.

REFERENCE


